

N-Channel Power MOSFET

60V, 300mA, 2Ω

FEATURES

- Low On-Resistance
- ESD Protected 2KV
- High Speed Switching
- Low Voltage Drive

KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
V_{DS}		60	V	
R _{DS(on)} (max)	$V_{GS} = 10V$	2	0	
	$V_{GS} = 4.5V$	4	Ω	
Q_g		0.4	nC	

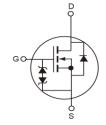
APPLICATION

- Logic Level translators
- DC-DC Converter









Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	60	V	
Gate-Source Voltage		V_{GS}	±20	V	
Continuous Drain Current (Note 1)	$T_A = 25^{\circ}C$	l _D	300	mA	
	T _A = 100°C		180		
Pulsed Drain Current (Note 2)		I _{DM}	800	mA	
Total Power Dissipation @ T _A = 25°C		P _{DTOT}	300	mW	
Single Pulsed Avalanche Energy (Note 3)		E _{AS}	0.2	mJ	
Single Pulsed Avalanche Current (Note 3)		I _{AS}	2	А	
Operating Junction and Storage Temperature	e Range	T_J, T_STG	- 55 to +150	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	350	°C/W	

Notes: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 PCB in still air



ELECTRICAL SPECIFICATIONS (T _A = 25°C unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT	
Static (Note 4)							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\mu A$	BV _{DSS}	60			V	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	$V_{GS(TH)}$	1.0	1.5	2.5	V	
Gate Body Leakage	$V_{GS} = \pm 20V$, $V_{DS} = 0V$	I _{GSS}			±10	μA	
Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	I _{DSS}			1.0	μΑ	
Durin Co. Co. Chata Basista	V _{GS} =10V, I _D =300mA	1_		1.2	2	Ω	
Drain-Source On-State Resistance	V _{GS} =4.5V, I _D =200mA	R _{DS(ON)}		2	4		
Forward Transconductance	V _{DS} =10V, I _D =200mA	g _{fs}	100			mS	
Diode Forward Voltage	I _S =300mA, V _{GS} =0V	V _{SD}		0.8	1.4	V	
Dynamic (Note 5)	Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 10V, I_D = 250mA,$ $V_{GS} = 4.5V$	Q_g		0.4	0.6	nC	
Input Capacitance		C _{iss}		30			
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$	C _{oss}		6		pF	
Reverse Transfer Capacitance	f = 1.0MHz	C _{rss}		2.5			
Gate Resistance	F = 1MHz, open drain	R_{g}		70		Ω	
Switching (Note 6)							
Turn-On Delay Time	$V_{DD} = 30V, R_G = 10\Omega$	t _{d(on)}		25			
Turn-Off Delay Time	$I_D = 200 \text{mA}, V_{GEN} = 10 \text{V},$	t _{d(off)}		35		ns	
Source-Drain Diode (Note 4)							
Diode Forward Voltage	I _S =300mA, V _{GS} =0V	V _{SD}		0.8	1.4		
Reverse Recovery Time	I _S = 0.5A	t _{rr}		40		ns	
Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	Qrr		39		nC	

Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. L = 0.1 mH, $I_{AS} = 2A$, $V_{DD} = 25V$, $R_G = 25\Omega$, Starting $T_J = 25^{\circ}C$
- 4. Pulse test: PW \leq 300 μ s, duty cycle \leq 2%
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.



ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM2N7002KCX RFG	SOT-23	3,000pcs / 7" Reel

Note:

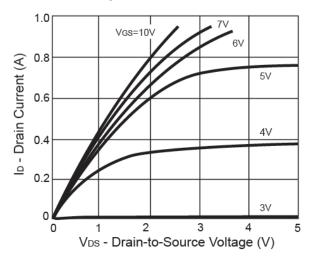
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition



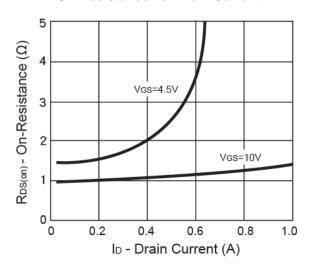
CHARACTERISTICS CURVES

(T_C = 25°C unless otherwise noted)

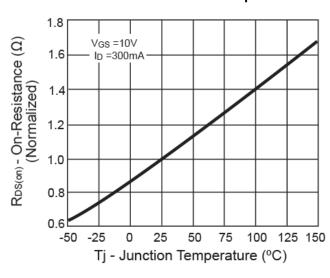
Output Characteristics



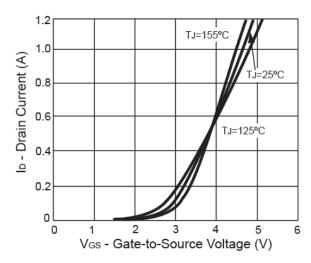
On-Resistance vs. Drain Current



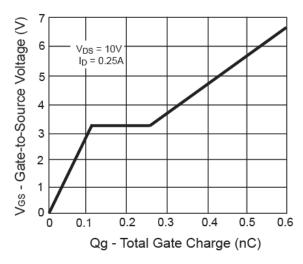
On-Resistance vs. Junction Temperature



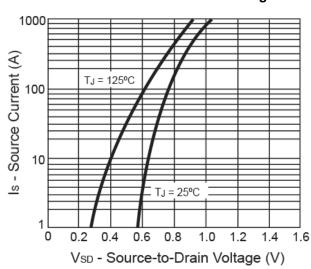
Transfer Characteristics



Gate Charge



Source-Drain Diode Forward Voltage

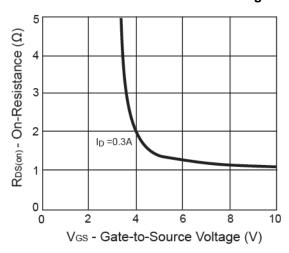




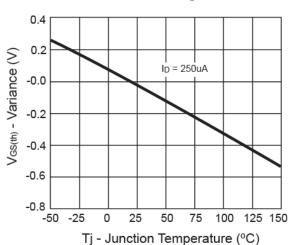
CHARACTERISTICS CURVES

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$

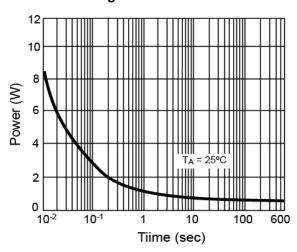
On-Resistance vs. Gate-Source Voltage



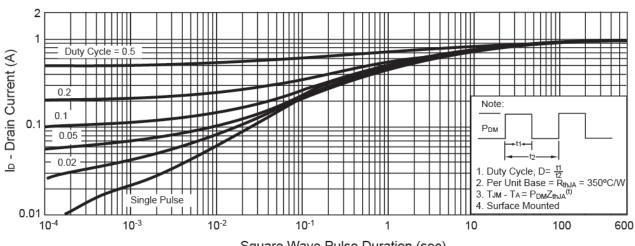
Threshold Voltage



Single Pulse Power



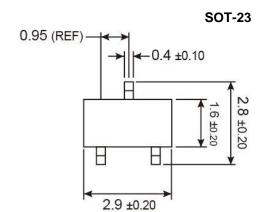
Normalized Thermal Transient Impedance, Junction-to-Ambient

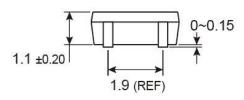


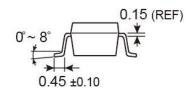
Square Wave Pulse Duration (sec)



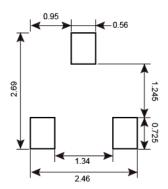
PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)



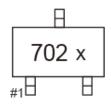




SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



702 = TSM2N7002KCX Device Code

X = Internal Code



Taiwan Semiconductor

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